UDP Offload Engine IP Core for FPGA

UOE IP Core for 10/25/50/100 GbE

- Future proof your application; optimize throughput for all line rates
- Operates at 10 GbE or 25 GbE; upgradable to 50/100 GbE
- Run full line rate with no packet loss, even for very small packets
- Offloads UDP standard RFC 768 from software to hardware
- Robust multicast support

Atomic Rules

The Atomic Rules UDP Offload Engine (UOE) IP Core allows for immediate operation at 10 or 25 GbE, while providing a simple path to 50/100 GbE.

The UOE IP core implements the UDP standard RFC 768, including checksum, segmentation and reassembly hardware offload. This offloads much of the work described in RFC 768 from software to hardware. In doing so, line rates of 25, 50, and 100 GbE are achievable.

The UOE IP core enables application-level UDP datagrams to be concurrently sent and received on a LAN or across a network. An integral IGMPv2 multicast pre-selector removes unwanted traffic, and L4 UDP multicasts are pre-selected so that user applications don't have to perform this function. The UOE IP core is tested for operation with popular FPGA vendors' 10 GbE and 25 GbE Ethernet MACs.

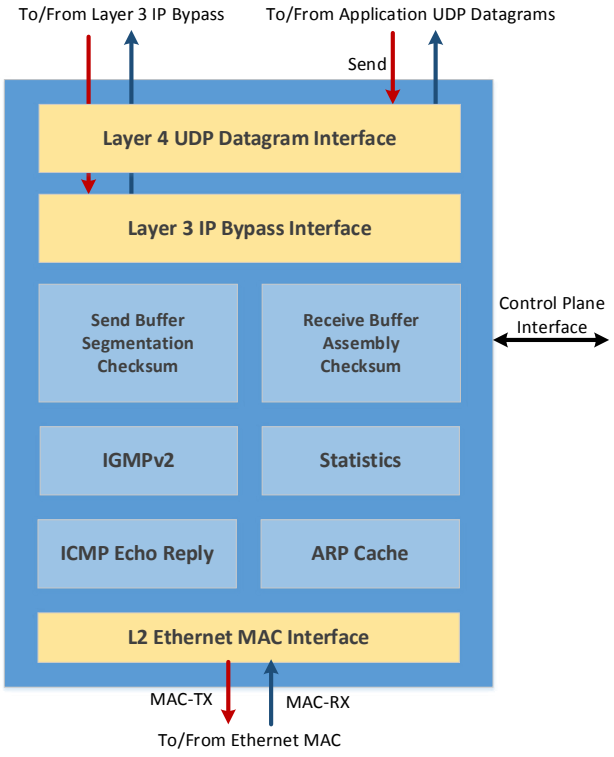
Product Operation

RTL sequential circuits in the UOE IP core handle the real-time interconversion of user datagrams and Ethernet frames. The core can function simultaneously as a UDP Sender and a UDP Receiver.

To send a datagram, the core is presented with a datagram and metadata describing the destination and port. If the MAC address for the destination IP address is unknown, the ARP circuit in the core resolves it. If the PDU of the datagram being sent exceeds the MTU, the core segments the datagram into fragments.

To receive , the core listens for Ethernet frames that encapsulate a UDP/IP payload. If the checksums are correct, it forms the datagram out of one or more fragments. When an entire datagram is ready, it is presented to the application logic along with its metadata.

When receiving multicast datagrams, the core preselects and delivers to the application only the host groups that have been joined by IGMP. This capability offloads the task of decoding the 2^{28} ClassD multicast addresses to a 4-bit code encoding 16 host groups.



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Detailed Feature List

- UDP/IPv4 (RFC 768, RFC 791)
- Hardware checksum, segmentation, and reassembly offload
- Multicast (IGMPv2) Capability
  - Join and leave support for receiving 16 Class-D groups
  - Send and receive multicast host groups
  - Receive pre-selecting offload (discard of unsubscribed multicasts)
- Concurrent datagram send and receive
- Ethernet packet: programmable frame MTU up to 16K Bytes (Super-Jumbo Frame support)
- UDP packet arbitrary datagram PDU up to IPv4 limit of 64K Bytes
- 16 Entry ARP cache (RFC 826)
- ICMP (unsegmented echo response message type only, used by "ping")
- VLAN (IEEE 802.1Q) support
- Layer 3 direct, allowing non-UDP application connectivity
- Statistics accessible by control-plane interface
- Low-Area implementation, allowing multiple core instances per FPGA
- Industry-standard AXI4 Interfaces (Avalon-Adapted on Altera devices)

Reference Designs

Atomic Rules offers UDP IP reference designs for both Altera and Xilinx FPGAs at 28 and 20 nm. Atomic Rules UOE IP Core can operate at up to 400 MHz in such cases where 25 GbE must be implemented with the smallest footprint possible. The data in the table below is typical.

Sample Implementation Results

Device / Size	Speed	ALMs / 6LUTs	FFs	BRAM	Fmax (MHz)	GbE
Arria V GZ E1/E7	C3	9,200	14,300	63 - M20K	156	10
Stratix V AB	C2	9,200	14,300	63 - M20K	156	10
Arria 10*	C2	18,000	20,000	65 - M20K	400	25
Virtex UltraScale	-2	18,000	20,000	22 - RAMB36	400	25

* Estimated utilizations and Fmax.

Deliverables

The IP core is available in encrypted or full source forms. Both versions include the elements needed for implementation, including a self-validating testbench. Most of the verification IP is also synthesizable, enabling testing to be performed at line rate, not just within a Verilog simulator.

Encrypted: The core is delivered as a collection of encrypted IEEE 1364-2005 Verilog RTL files.

Full Source: Contact BittWare or Atomic Rules for availability.

Ordering Information

Contact BittWare for details.

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